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VLSI BASED SELF HEALING SOLUTION FOR FAULT TOLERANT DIGITAL CIRCUITS

***Meyyappan, S. and Alamelumangai, V.**

Department of E&I Engg., Annamalai University, Annamalai Nagar 608002

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ABSTRACT

The paper endeavours to unveil a design strategy to retain the true nature of the output in the event of occurrence of faults at the interconnect level of cascaded digital circuits. The operational pattern of the combinational circuit facilitates the creation of a self healing attribute and ensures the reliability of the digital architecture. The proposed scheme inserts faults randomly into the system at the interconnect levels and fosters to predict its behaviour in response to a fault. The scheme be-hives the formation of a self checking mechanism to aid in the process of analysing the signals at different stages for both stuck at 0 and 1 faults. The design encompasses ways to intrigue the state of the intermediate signals and carries it with steps to rig out the true values at the primary output lines. The Modelsim based simulation results obtained for a decoder designated as the circuit under test emphasize the suitability of the scheme and avail the attributes of an FPGA to exhibit its practical viability.

INTRODUCTION

The performance of a digital system owes its competence to the selection of highly reliable components and the use of proven methods for their interconnection. The system requires an extensive verification of the logic design, programs and final hardware using simulation, diagnostic and functional tests in the expected environmental conditions. In spite of these reliability assurance techniques, the system may still fail during normal operation due to uncontrollable or undetectable faults. These are caused by undetected design errors, random failures of components or connections, and externally induced malfunctions during the operation of the system. An immediate way to cope up with faults in digital systems leads to incorporate fault tolerance thereby restoring the normal operation of the system even in the presence of faults (Lala, 2012 and 2001]. The complexity of present-day VLSI devices continues to rise and the chips are therefore becoming untestable by external Automated Test Equipments (ATE) (Lala *et al*., 2003) and (Lala *et al*., 2006). The test lengths appear to rapidly increase in line with the testing times and the ATE memory requirements, in light of which the Built-In Self-Test (BIST) establishes itself as a necessary part of VLSI circuits.

****Corresponding author:** *Meyyappan, S***
Department of E&I Engg., Annamalai University, Annamalai Nagar 608002

The circuit equips with it to test itself by BIST without using any ATE equipment or when used together with an external tester. The BIST is an on-chip testing system that generates test vectors to detect faults and elongates to verify the fault prone nature of the hard-ware. A fault injection system provides the capability to induce a fault at any desired location and the philosophy allows faults to be injected at varying hierarchial levels of the testable system. The process of fault injection appears to be crucial in any digital measurement system. It enables the designer to introduce faults in the connecting lines to arbitrate on the need for a self healing strategy in order to make it fault tolerant. The faults in a testable system are assumed to be mainly single bit faults where a single bit is flipped from logic 1 to a 0 or vice-versa.

The theory of fault injection relates to the intentional insertion of faults into a system for the purpose of studying its response. The techniques for fault injection fall into three categories: (i) simulation based fault injection in which fault is injected into the simulation models of systems, (ii) software implemented fault injection that contains fault injection module in the VHDL description itself and (iii) physical fault injection capable of injecting faults into physical systems. The advantage of simulation-based fault injection extends to the fact that it can be used early in the design cycle. However, the main drawback to simulation-based fault injection lies in the context that it is time-consuming and the associated overhead limits the extent of usage, while injecting faults in the VHDL

description offers many advantages that include platform independence and portability among design packages. A realistic fault injection system necessitates the capability to access most signals within the VHDL format including the inputs and outputs of the description which is crucial for both on- and off-line testing.

A detailed survey on fault injection techniques has been carried out in (Haissam Ziade *et al*., 2004) with a purpose to bring out the relative merits and demerits of the various methodologies developed to inject faults into a system prototype or model. A probabilistic model has been developed in (Trailokya Nath Sasamal and Anand Mohan, 2011) to derive the optimum faulty period in a digital system. The faults with transient nature have been injected using VHDL program and the results used to validate the distribution functions in the model. A transient fault injection has been outlined at the VHDL level in (Lala, 2012), to establish its ability to evaluate the testability for digital circuits. An FPGA based fault injection tool that supports synthesizable fault models of digital circuits have been implemented using VHDL in (Swathi Rudrakshi *et al*., 2012). The design has been validated using state machine based examples for different types of faults. A circuit instrumentation approach has been adopted in (Civera, 2001) to inject faults in the system emulated to FPGA. The effectiveness of fault injection environment has been tested to provide speed up factors over other fault injection techniques.

A switch architecture for concurrent testing and diagnosis for faults in multistage interconnection networks has been proposed in (Minsu Choi, 2003). The compound effect of fault tolerant operation has been evaluated and the results show graceful performance enhancement due to fault tolerance. A partially self checking scheme for combinational circuits with concurrent error detection facility has been presented in (KShirsagar, 2007). The results have been related to significantly reduce the area overhead in two level circuits. An FPGA architecture that is composed of functional cells has been discussed in (Lala, 2008) to bring out its error correction capabilities. An architecture that enables tolerance of single bit errors in a functional cell of the FPGA has been presented. The occurrence of faults relate to unpredictable changes in the components of a logic circuit and permanently alter the logic function in the sense it may lead to deviations from the specified values of logic variables. Thus, an astute fault generator along with a facility to arrive at the correct state of the variable is of crucial significance to ensure the dedicated purpose of the digital system in use. The paper houses four major divisions which explain the formulation procedure, simulation results, experimental elucidation and end with concluding comments.

MATERIALS AND METHODS

The main focus corners to formulate a sequence with a view to inject faults in the lines that interconnect the combinational circuits in a digital system. It examines the signal status to articulate a healing sense and there from arrive at the error free value of the measured variable. The generation of test patterns strive to offer formidable strength in realizing the correct state at the output of the system. The scheme derives the benefits of the Modelsim platform to implement the methodology on a Spartan board to eschew its applicability in the practical world. A key factor in the design of fault-tolerant digital systems owes its ability to address issues of dependability requirements. The fault injection defines itself to be an effective method to study error behaviour, measure the dependability parameters and evaluate fault-tolerant digital systems. Traditionally, highly critical applications rely on hardware redundancy to increase their reliability. The best known Triple Modular Redundancy (TMR) achieves fault tolerance without actually detecting any fault. In this method, each module, which may be a complete system, such as a computer, or a less complex unit, like a microprocessor or even an adder or a gate replicates itself three times. The voting element collects the outputs from the three sources and delivers the majority vote at its output.

The choice of a decoder as Circuit Under Test (CUT) owes to its exclusive dependence in any digital measuring environment and the fact that the philosophy can easily relate to other circuits. The Fig. 1 illustrates the details of the constituent components of the fault tolerant decoder that serve to insert, deduce and heal the occurrence of possible faults. It includes as many numbers of decoders along with a reference unit that cascade with suitable number of ex-or gates, priority encoders and multiplexers to retrieve the truthful output. The ex-or gates along with the priority encoders stretch to select the appropriate line from the similar decoder outputs for the multiplexer where from the sequence acquires the correct output. The incorporation of the reference module assuages to trace the corrective nature of the variable and resurrect the stuck nature of the intermediate signal. The theory of Linear Feedback Shift Registers (LFSR) treads to generate pseudo-random numbers that can be used as test patterns in logic circuit testing. The outputs of a selected number of stages in a shift register connected to its input through an EX-OR network form the LFSR. The output of any stage results as a function of the initial state of the bits in the register and of the outputs of the fed back states. The selection of feedback paths thus becomes crucial in the construction of an LFSR to allow it to perform in tune with the design. The Fig. 2 shows the general representation of an LFSR based on the primitive polynomial given below.

$$P(x) = x^n + p_{n-1}x^{n-1} + \ldots + p_2x^2 + p_1x + p0$$

The methodology explained using the flow diagram in Fig. 3 pronounces a procedure to inherently introduce faults in more than one interconnect levels of the test circuit and interleave out a self healing stream to arrive at a fault tolerant digital system. The self healing mechanism revolves around the use of a reference module to articulate the true output. The function of a LFSR adds to introduce faults in the intermediate lines and bring out the random nature of the occurrence of faults in a real time environment. The creation of test patterns adds a new dimension to the approach in the sense it forges the unintended nature of the behaviour of the digital systems and carries the mechanism to perform correctly even under extraneous circumstances.

RESULTS

The modern digital systems experience the merits in the use of high level language such as VHDL.

The actual implementation of the system follows the specification and reverberate the need for the compliance of testability, power consumption and a sense of reliability. The ability to simulate the occurrence of a fault in the VHDL description of a circuit assumes extreme importance to heave the circuit with a built-in on-line fault detection capability. The internal signal requires to be accessed at the VHDL level for the purposes of injecting faults to ensure greater coordinative characteristics for the system (Luis Entrena, 2001).

The scheme involves the use of two decoders together with a reference mandate and orients to connect the LFSR either at the first or the second decoder to realize the natural introduction of faults at the different intermediate levels of the test system. The fundamental operating mechanism of the constituent digital circuits embody the formulation of the tolerant mechanism and offer the desired value of the output for any combination of the digital states. The strategy avails the role of Modelsim platform to illustrate the veracities through VHDL description.

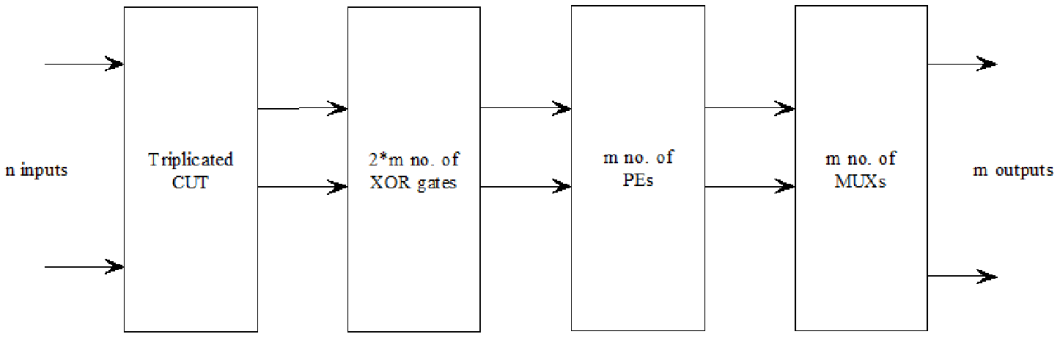

Fig. 1 lock diagram of the self healing decoder

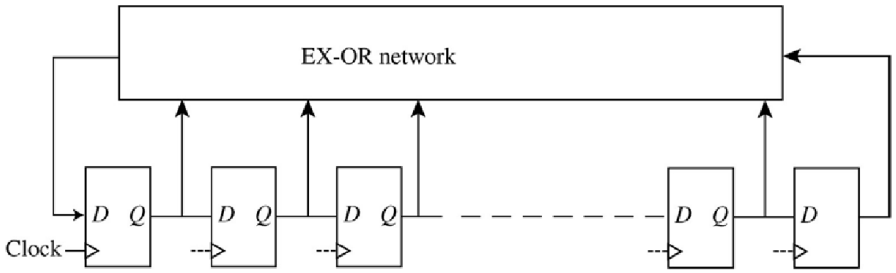

Fig. 1 Block diagram of the self healing decoder

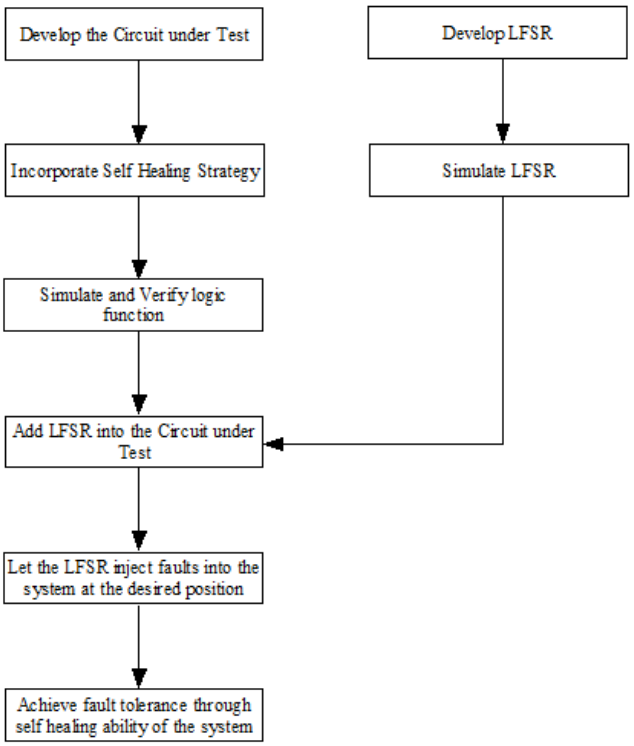

Fig. 3. low diagram of the fault tolerant design

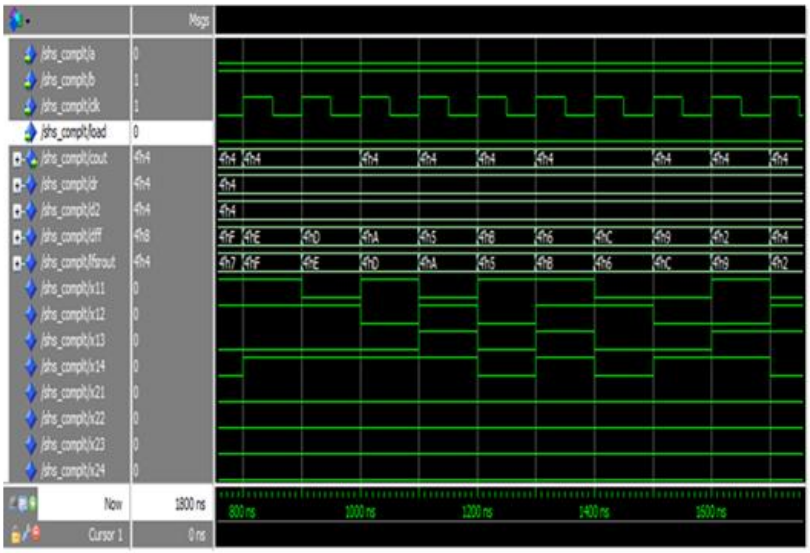

Fig. 4. Output of the self healing system with faults in the output lines of the first decoder

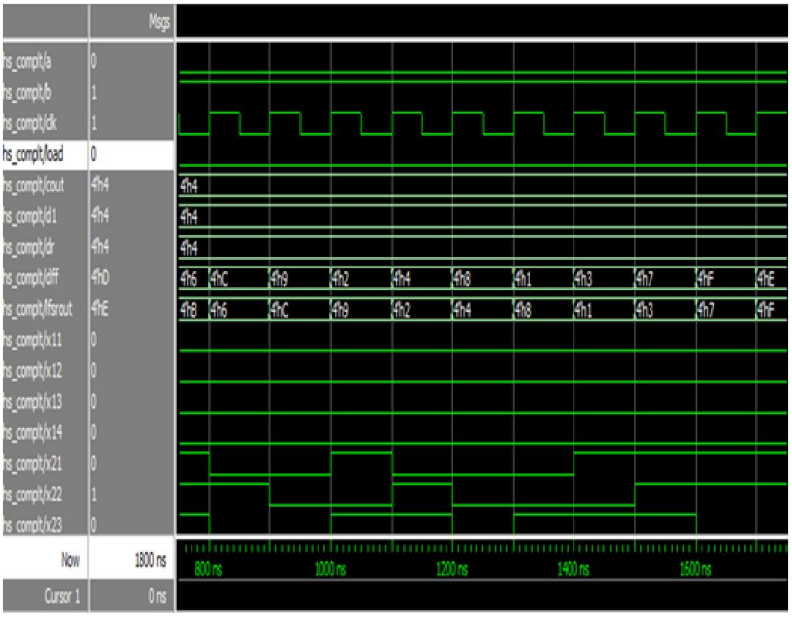

Fig. 5. Output of the self healing system with faults in the output lines of the second decoder

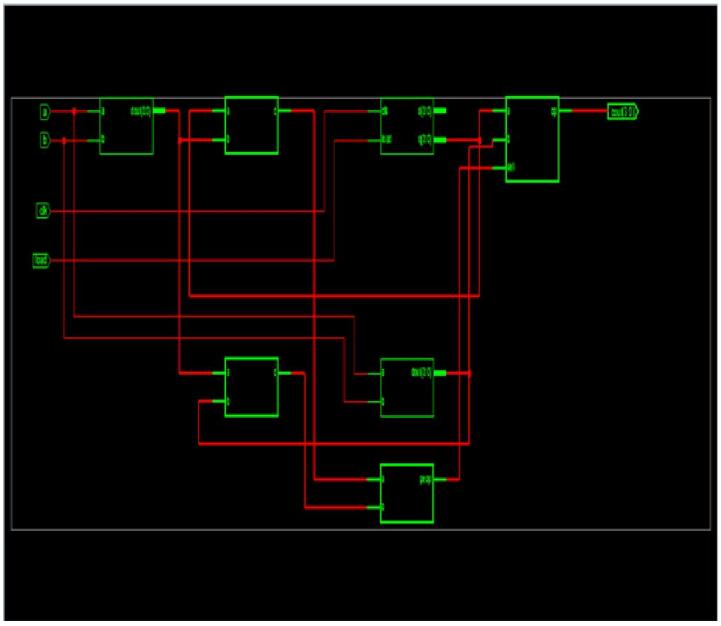

Fig. 6. RTL schematic of the fault tolerant system

The signals seen in Figs. 4 and 5 relate to the outputs of the LFSR connected in place of the decoders, the intermediate and final outputs over a sequence of clock cycles. The LFSR outputs project the ability of the design to randomly bring in faults at all the intermediate levels and still ensure the correct output of the system. The Figs. 4 and 5 respectively correlate to LFSR replacing first and second decoders with different seed values.

Hardware Implementation

Hardware redundancy appears to be a preferred choice to support the reliability of highly critical applications in this field. FPGAs in light of their inherent configurability and function independent stature acclaim its suitability for the implementation of modular redundancy (KShirsagar, 2007) and (KShirsagar, 2008). The FPGAs replicate the emergence of reconfigurable computing systems and reap the benefits of new process technologies owing to which it becomes the preferred choice over today's discrete devices.

The RTL schematic shown in Fig. 6 displays the components that constitute the self healing architecture along with a fault generator in the form of LFSR. The XC3S500E FPGA synthesizes the VHDL code generated to realize the fault tolerant design on the Xilinx Foundation 9.2.i platform. The very fact that it assuages a synthesizable code serves to validate the cohesive nature of the strategy and authenticates the use of the proposed approach for tracing the real output in the event of fault interruptions in a digital system.

Conclusion

The artefacts of the basic operational theory have been eschewed to articulate a self healing solution for combinational digital circuits. The nuances of LFSR have been incorporated to create test patterns at the different intermediate levels of the three stage cascaded structure. The formulation has been enlivened through the natural introduction of faults on one or more lines over which the signal flows. The Modelsim based simulation results have been obtained from the VHDL code tailor made to trace the fault free output for the multiple combinations of testable patterns in the chosen decoder circuit under test. The capabilities of XC3S500E FPGA have been sought to encrypt a synthesizable RTL circuitry and encompass an environment suitable to validate the proposed scheme. The inert facility to address interconnect faults in the chosen digital architecture has been focussed to reiterate the fault tolerant aspect and acclaim for itself a wider spectrum of use in a band of digital circuit related paraphernalia.

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