



Full Length Research Article

SYMMETRICAL MULTILEVEL INVERTER WITH HYBRID PWM STRATEGIES

¹Nithya, S., ²Balamurugan, C. R., ³Natarajan, S. P.

^{1,2}Department of EEE, Arunai Engineering College, Tiruvannamalai, Tamilnadu, India

³Department of EIE, Annamalai University, Chidambaram, Tamilnadu, India

ARTICLE INFO

Article History:

Received 08th January, 2014
Received in revised form
11th February, 2014
Accepted 15th February, 2014
Published online 14th March, 2014

Key words:

PD, APOD, VF, CO,
SINETRAP and
PWM

ABSTRACT

In this paper various new hybrid PWM strategies for sine-trapezoidal reference with triangular carrier PWM signals are analyzed with the new symmetrical nine level inverter topology. This new multilevel level inverter uses only ten switches rather than conventional multilevel inverter uses sixteen switches for the same nine level output. The topology has many advantages of less switching losses, converter cost and installation cost. The inverter is analysed with PWM strategies like PD, APOD and also with various new hybrid PWM strategies such as PD + VF, PD + CO, APOD + VF, APOD + CO, PD + VF + CO and APOD + VF + CO. The proposed multilevel inverter is investigated with these techniques in MATLAB/SIMULINK. The power quality issues such as Total Harmonics Distortion and Fundamental RMS voltages are analysed by comparing this strategy. As a result, the total harmonic distortion is lower in PD + VF PWM strategy and fundamental RMS voltage is higher in APOD + VF + CO PWM strategy.

Copyright © 2014 Nithya et al. This is an open access article distributed under the Creative Commons Attribution License, which permits unrestricted use, distribution, and reproduction in any medium, provided the original work is properly cited.

INTRODUCTION

The multilevel converter has been introduced since 1975. Generally inverter is defined as a device which converts DC power to AC power at desired output voltage and frequency. Less efficiency, high cost and high switching losses are disadvantages of this inverter. These demerits are overcome by using multilevel inverter. The term multilevel states that power conversion are produced by utilizing multiple small voltage levels. Small voltage step results in making the multilevel inverter withstand better voltage, fewer harmonics, lower switching losses, good electromagnetic compatibility, higher voltage capability and better power quality. This multilevel inverter produces output voltage in staircase shape which looks like a sinusoidal waveform. Various applications of multilevel inverters are renewable sources, industrial drives, laminators, blowers, fans and conveyors. In those applications voltage ranges from medium to high level. If the output of the multilevel inverter is increased by N level, then the harmonics of the output voltage is reduced to zero. Cascaded multilevel inverter was developed in initial stage. In second stage diode clamped multilevel inverter and later flying capacitor was introduced. These three topologies utilise different mechanism to produce requires output.

Among these three topologies, cascaded multilevel inverter has more advantages such as simple construction using less number of switches, no need of clamping diode, flying capacitor and absences of voltage unbalance. Most of the researches are carried out in cascaded multilevel inverter configuration. But still the new trends are involved in the evolution of renewed multilevel inverters. Modifications are made in its inbuilt structure. In this paper, a 9-level MLI is generated with 10 switches, by reducing 6 switches from the main conventional MLI. Rao *et al.* (2013) presents a new class of three phase seven level inverter based on a multilevel DC link and a bridge inverter to reduce the number of switches. Deepak *et al.* (2013) proposes a new concept of switching with reduced number of switches and batteries, it helps to reduce the complexity of switching and DC link counterparts. Jamuna *et al.* (2012) emphasis a asymmetrical multilevel inverter with multiple trapezoidal PWM and multiple sinusoidal PWM technique with triangular as carrier. Farokhnia *et al.* (2012) study on modified SHE-PWM technique that extends the standard modulation region and generates a stepped waveform. Lakshmi *et al.* (2012) made a performance on symmetrical and asymmetrical inverter. Chithra *et al.* (2011) carried out a analysis on symmetrical and asymmetrical single phase CHB multilevel inverter with respect to harmonics content. Palanivel *et al.* (2011) various carrier pulse width modulation techniques are proposed, which can minimise the total harmonic distortion and enhances the output voltage from 5-levels inverter. Kadir *et al.* (2009) presents a multilevel

***Corresponding author: Balamurugan, C. R.,**
Department of EEE, Arunai Engineering College, Tiruvannamalai,
Tamilnadu, India

multistage inverter design and its corresponding control strategy to ensure minimum switching losses focusing on holding the higher voltage stage state as long as it is feasible. Panagis et al. (2008) introduced a comparison between existing state of the art multilevel inverter topologies such as NPCMLI, DCMLI, FCMLI and the CCMLI are performed. In-Dong Kim et al. (2004) proposed snubber circuit makes use of an undeland snubber as a basic snubber unit. Poh Chiang Loh et al. (2003) deal a modulation strategy for cascaded multilevel inverters that substantially eliminate common-mode voltage on the output phases. Rodriguez et al. (2002) describes the most relevant control and modulation methods for multilevel sinusoidal pulse width modulation, multilevel selective harmonic elimination and space-vector modulation.

Conventional Cascaded Multilevel inverter Topology

Fig. 1 shows the conventional 9-level cascaded multilevel inverter topology. It requires 4 DC sources and 16 switching devices. It produces nine level output of $4V_{dc}$, $3V_{dc}$, $2V_{dc}$, V_{dc} , 0 , $-V_{dc}$, $-2V_{dc}$, $-3V_{dc}$ and $-4V_{dc}$. The switching table for nine level cascaded multilevel inverter in table1. The load is connected between terminal A and N.

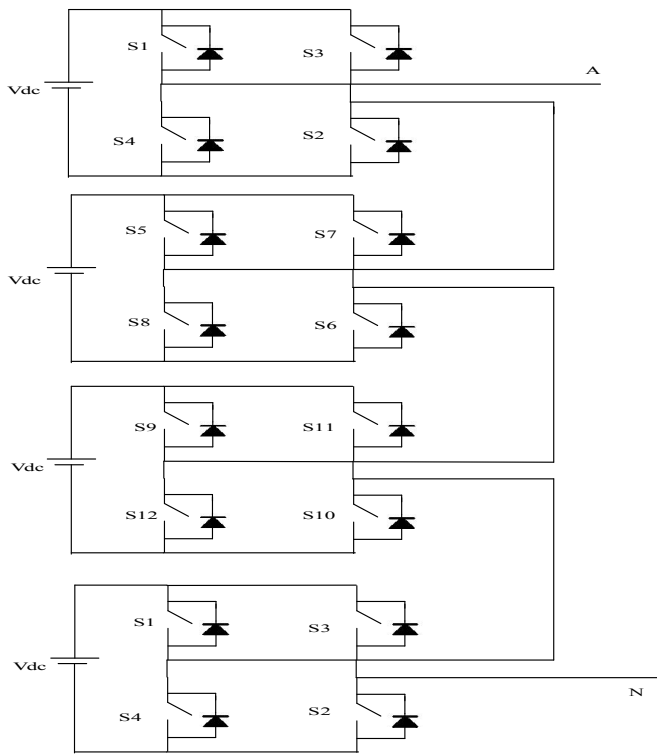


Fig. 1. Block Diagram of Conventional Symmetrical 9- Level Inverter

Construction and Operation of Proposed Topology

Aiming at reducing the switches to the maximum possible extent and reducing complexity, the new topology is introduced with ten switches for nine levels. This new MLI configuration is made of 10 switches eliminating six switches from the existing conventional topology with four equal input DC sources to produce nine level output. Then the concept of “Switch Reduction” is introduced. The fewer switches we use, that reduces the cost of circuit building. MOSFETs were used for the switching devices. As a practical scenario, switching

the series MOSFETs so that they dynamically share the bus voltage is a major challenge. The inverter produces output voltage in nine levels: $4V_{dc}$, $3V_{dc}$, $2V_{dc}$, V_{dc} , 0 , $-V_{dc}$, $-2V_{dc}$, $-3V_{dc}$ and $-4V_{dc}$. This multilevel inverter has main four advantages than the conventional inverter. First, the voltage stress on each switch is decreased due to series connection of the switches. Therefore, the rated voltage and consequently the total power of the inverter could be safely increased. Second, the rate of change of voltage (dv/dt) is decreased due to the lower voltage swing of each switching cycle. Third, harmonic distortion is reduced due to more output levels. Fourth, lower acoustic noise and electromagnetic interference (EMI) is obtained.

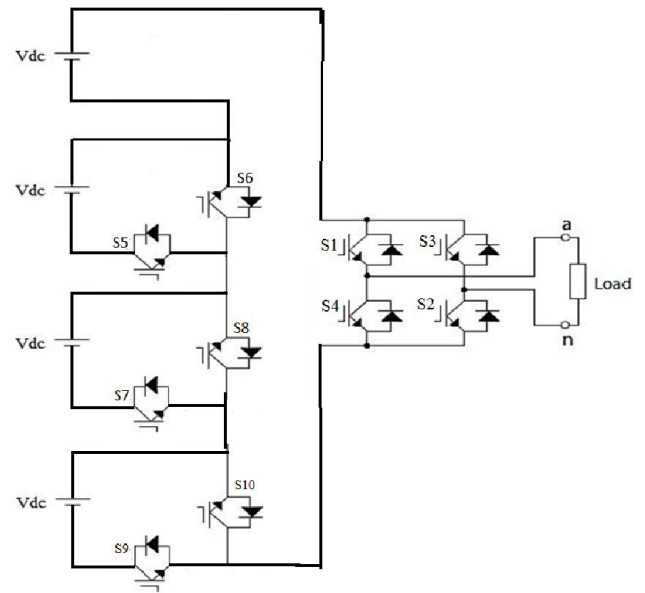


Fig. 2. Proposed Symmetrical 9- Level Inverter

Figure 3 shows the output voltage waveform for the symmetrical 9-level proposed inverter.

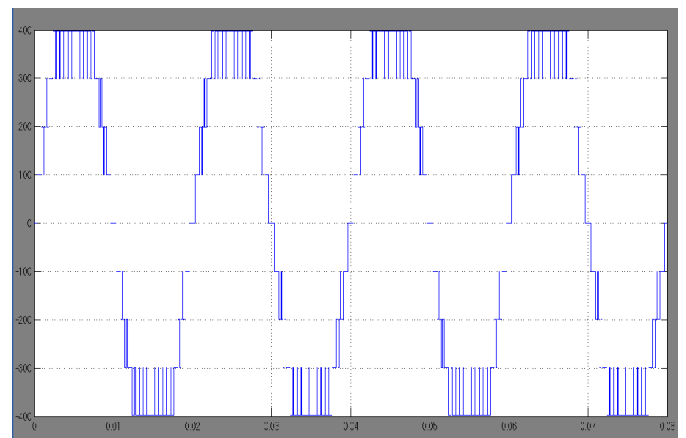


Fig. 3. Nine-Level Output for the Proposed Inverter

Simulation for Various Hybrid PWM Strategies with Sine-Trip Reference and Triangular Carrier Signal

In this proposed work a unipolar strategy is used to generate firing pulses for a seven level inverter. For an M-level inverter using unipolar multicarrier technique, (m-1)/2 carriers with the same peak-to-peak amplitude A_c and same frequency f_c are used. The reference wave is continuously compared with each

of the carrier signal, and then the active devices corresponding to that carrier are switched on. Otherwise, the device is switched off. The reference signal is taken as the hybrid SINE-TRAP signal and it is the sum of sinusoidal and trapezoidal signals. The carrier signal is triangular signal. Carriers needed for m level is m-1 in conventional strategies, but for unipolar PWM strategies [(m-1)/2]. Therefore for nine levels, only four carrier signals are required.

Phase Disposition Strategy

In this method all the carriers are have the same frequency, same amplitude and same phase. All carriers selected above and below the zero reference are in same phase and amplitude of each carrier is chosen as 1. Since all carriers are in same phase it is named as Phase Disposition PWM (PDPWM). Amplitude Modulation for this strategy is defined as:

$$m_a = \frac{A_m}{n * A_c}$$

Where n is the number of carriers used to generate seven levels.

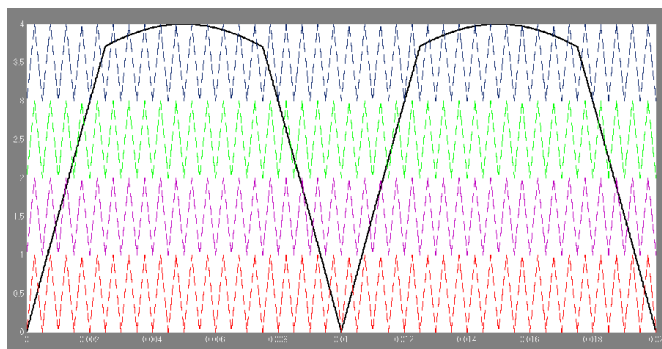


Fig. 4. PD PWM Strategy for SINE-TRAP Reference with Triangular Carrier Signal

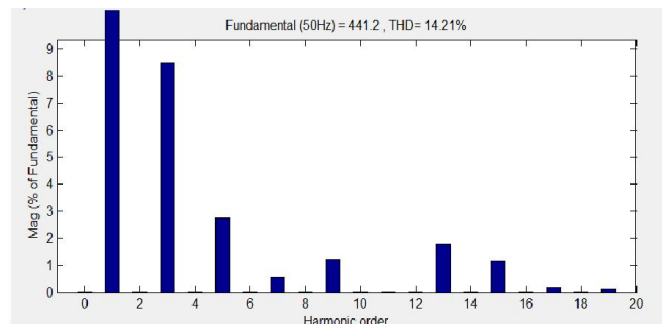


Fig. 5. FFT Plot Analysis for PD PWM Strategy

Alternate Phase Opposition Disposition Strategy:

In this strategy, carries are seem to be invert their phase in turns from previous one so it is named as Alternate Phase Opposition Disposition PWM (APODPWM) strategy. Carrier set placed above the zero reference with Amplitude Modulation index for this strategy is defined as:

$$m_a = \frac{A_m}{n * A_c}$$

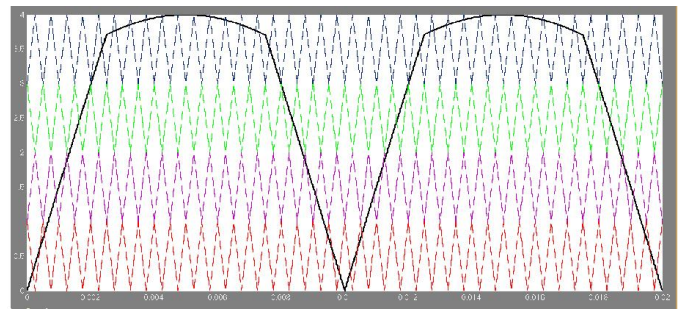


Fig. 6. APODPWM Strategy for SINE-TRAP Reference with Triangular Carrier Signal

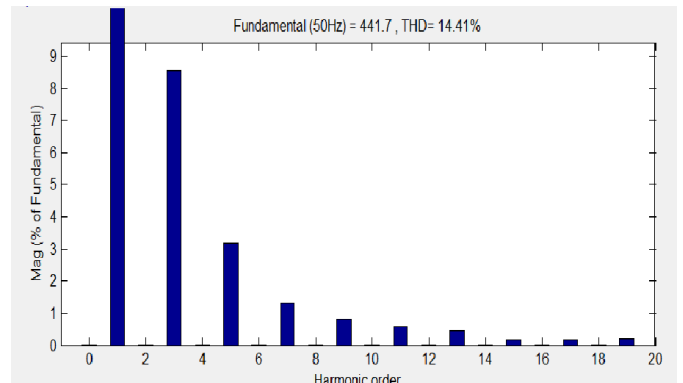


Fig. 7. FFT Plot Analysis for APODPWM Strategy

Phase Disposition + Variable Frequency (PD + VF) Strategy

In this technique, the entire carriers are in phase with each other but having variable frequency. So it is named as PD + VF PWM strategy. This technique will results in lesser harmonic distortion

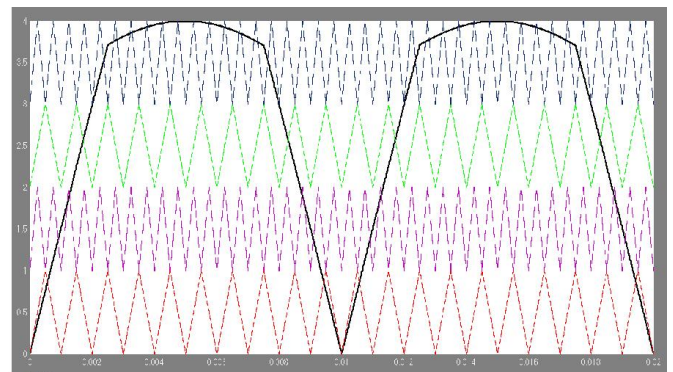


Fig. 8. PD + VF PWM Strategy for SINE-TRAP Reference with Triangular Carrier Signal

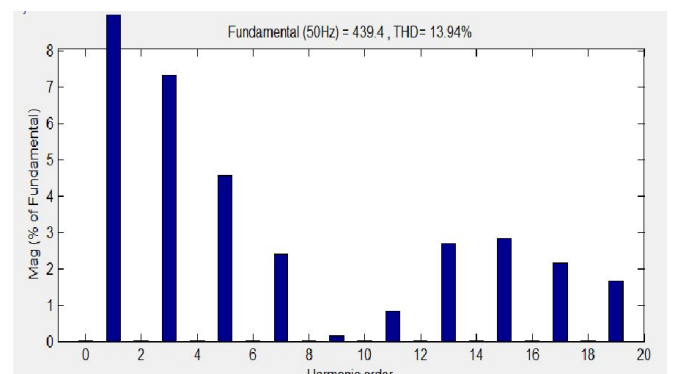


Fig. 9. FFT Plot Analysis for PD + VF PWM Strategy

Phase Disposition + Carrier Overlapping (PD + CO) Strategy

In this technique, the entire carriers are in phase with each other and having same frequency but all the carriers are overlapped with each other. So it is named as PD + VF PWM strategy. The reference signals is taken as SINE-TRAP signal, it is the combination of sinusoidal and trapezoidal signals. Comparison on various hybrid reference signals, this SINE-TRAP signal produces less total harmonic distortion. And also the carrier is chosen as triangular signal.

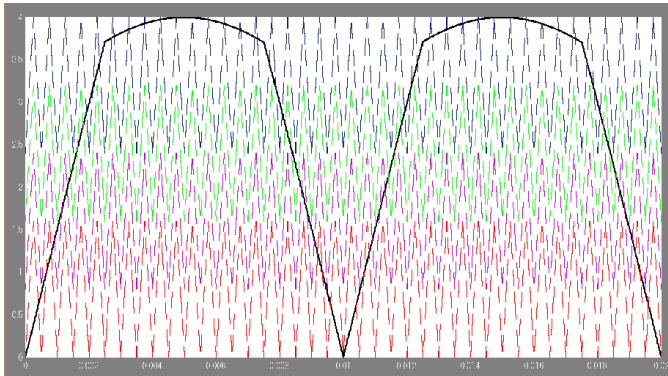


Fig. 10. PD + CO PWM Strategy for SINE-TRAP Reference with Triangular Carrier Signal

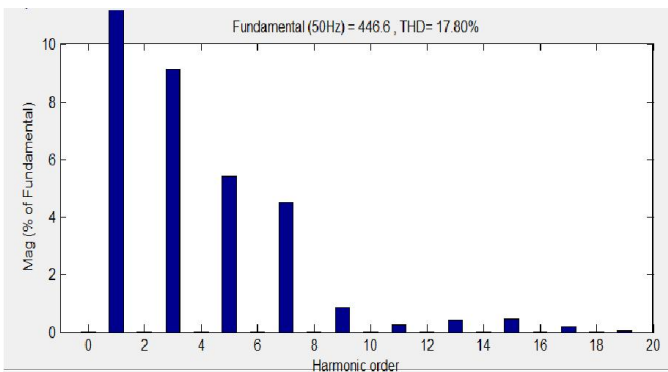


Fig. 11. FFT Plot Analysis for PD + CO PWM Strategy

Alternate Phase Opposition Disposition + Variable Frequency (APOD +VF) Strategy

In this technique, all carrier signals are having variable frequency and also they are invert in phase with the previous one. So it is named as APOD + VF PWM strategy.

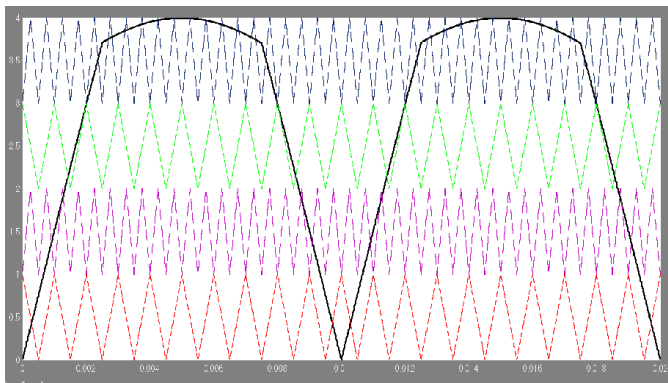


Fig. 12. APOD + VF PWM Strategy for SINE-TRAP Reference with Triangular Carrier Signal

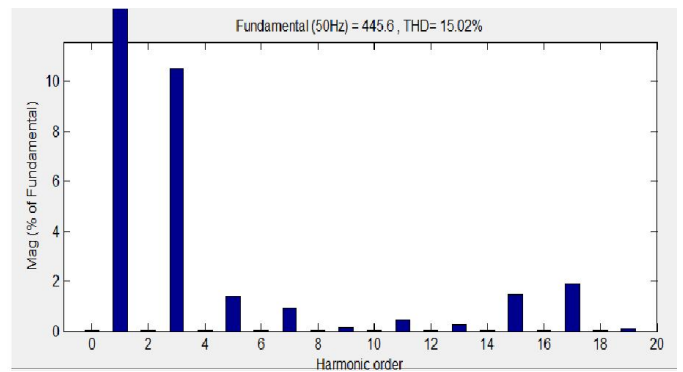


Fig. 13. FFT Plot Analysis for APOD + VF PWM Strategy

Alternate Phase Opposition Disposition + Carrier Overlapping (APOD +CO) Strategy

In this technique, all carrier signals having same frequency but all are overlapped with each other and also they are invert in phase with the previous one. So it is named as APOD + CO PWM strategy.

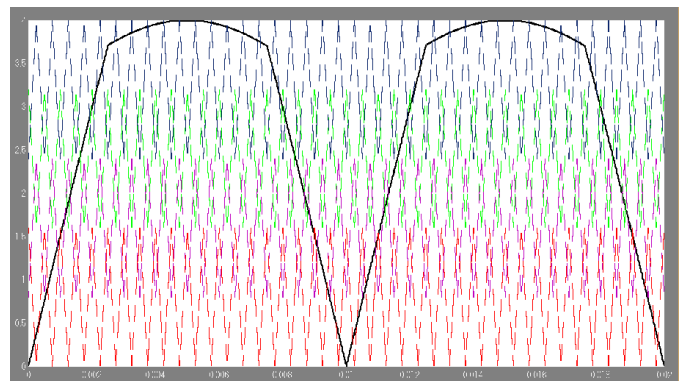


Fig. 14. APOD + CO PWM Strategy for SINE-TRAP Reference with Triangular Carrier Signal

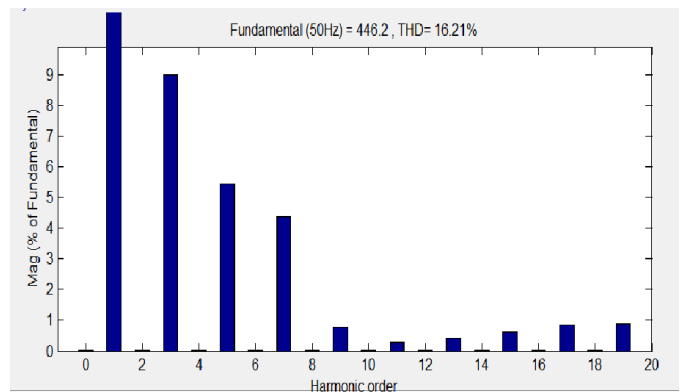


Fig. 15. FFT Plot Analysis for APOD + CO PWM Strategy

Phase Disposition + Carrier Overlapping + Variable Frequency (PD +CO +VF) Strategy

In this hybrid technique, Carrier signal 1 and 3 have variable frequency and all carrier signals are overlapped with each other and also they are in phase with the previous one. So it is named as PD + CO + VF PWM strategy.

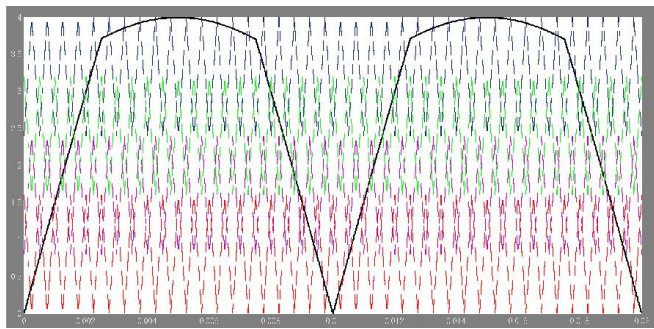


Fig. 16. PD + CO + VF PWM Strategy for SINE-TRAP Reference with Triangular Carrier Signal

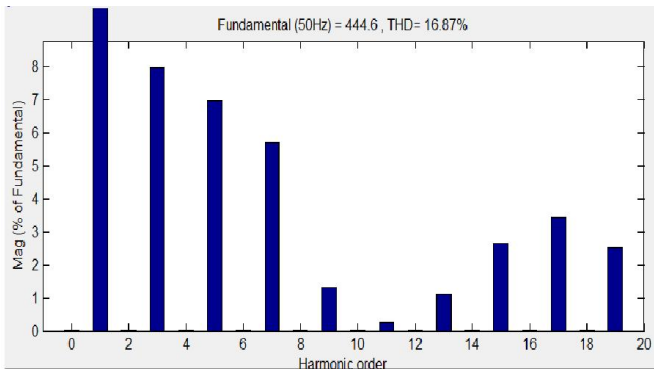


Fig. 17. FFT Plot Analysis for PD + CO + VF PWM Strategy

Alternate Phase Opposition Disposition + Carrier Overlapping + Variable Frequency (APOD + CO + VF) Strategy

In this hybrid technique, Carrier signal 1 and 3 have variable frequency and all carrier signals are overlapped with each other and also they are invert in phase with the previous one. So it is named as APOD + CO + VF PWM strategy. This technique will results in higher fundamental RMS voltage.

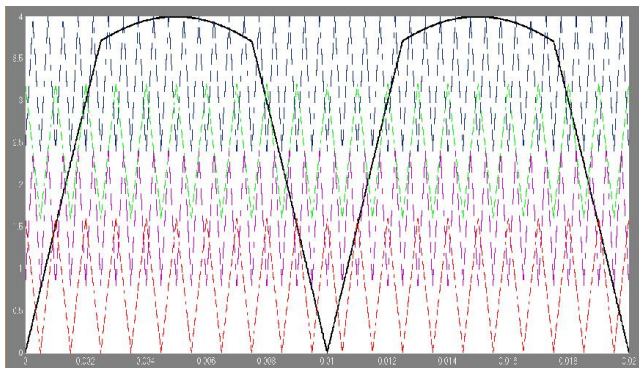


Fig. 18. APOD + CO + VF PWM Strategy for SINE-TRAP Reference with Triangular Carrier Signal

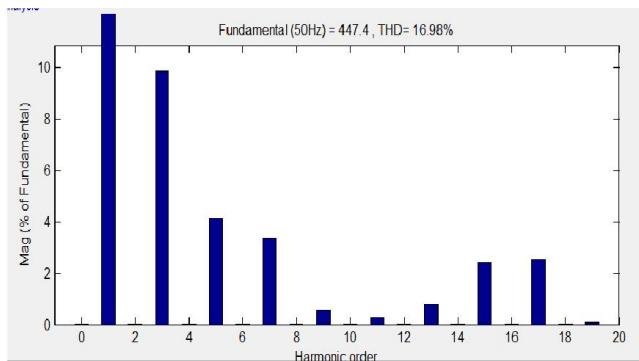


Fig. 19. FFT Plot Analysis for APOD + CO + VF PWM Strategy

Conclusions

The 9-level MLI using just ten switches is successfully introduced simulating the circuitry using MATLAB/SIMULINK and observed a clear stepped 9-level waveform. It is found that the SINETRAP reference with triangular carrier dominates all other combination of reference with carrier in the proposed configuration. The PD + VF PWM strategy produces the very less THD and APOD + VF + CO PWM strategy produces higher fundamental RMS output voltage. The new design is simple in its outlook with very few components. The novel 7-level multilevel inverter has lower THD compared to conventional symmetric and asymmetric topologies.

REFERENCES

Rao, S. N., D. V. A. Kumar and C. S. Babu, "New multilevel inverter topology with reduced number of switches using advanced modulation strategies," *IEEE Conf. Rec.*: 978-1-4673-6027-2, Feb 2013, pp. 693-699.

Deepak, R., V.S. Kasturi, L. Sarkar and Y. R. Manjunatha, "Novel multilevel inverter with reduced number of switches and batteries," *IEEE conf. Rec.*: 978-1-4799-1599-6, Dec 2013, pp.1-5.

Jamuna, P., and C. C. A. Rajan, "MSPWM & MTPWM techniques for asymmetric H-bridge multilevel inverter," *IEEE Conf. Rec.*: 978-1-4673-0213-5, Mar 2012, pp. 501-504.

Farokhnia, N., S. H. Fathi, R. Salehi and G.B. Gharehpetian, "Improved selective harmonic elimination pulse-width modulation strategy in multilevel inverters," *IET Trans. Power Electron.*, vol.5, no.9, pp.1904-1911, Nov 2012.

Lakshmi Ganesh, K., U. Chandra Rao, "Performance of Symmetrical and Asymmetrical Multilevel Inverters," *International Journal of Modern Engineering Research*, ISSN: 2249-6645, vol.2, no. 4, 2012, pp.2293-2302.

Chithra, M. and S. G. B. Dasan, "Analysis of cascaded H bridge multilevel inverters with photovoltaic arrays," *IEEE Conf. Rec.*: 978-1-4244-7923-8, Mar 2011, pp. 442-447.

Palanivel, P. and S. S. Dash, "Analysis of THD and output voltage performance for cascaded multilevel inverter using carrier pulse width modulation techniques," *IET Trans. Power Electron*, vol.4, no.8, pp.951-958, Sep 2011.

Kadir, M. N. A., S. Mekhlif and Hew Wei Ping, "Novel control strategy for three-stage 18-level hybrid multilevel inverter," *IEEE conf. Rec.*: 978-1-4244-4345-1, Mar 2009, pp.1-6.

Panagis, P., F. Stergiopoulos, P. Marabeas and S. Manias, "Comparison of state of the art multilevel inverters," *IEEE Conf. Rec.*: 978-1-4244-1667-7, Jun 2008, pp. 4296-4301.

In-Dong Kim, Eui-Cheol Nho, Heung-Geun Kim and Jong Sun Ko, "A generalized undeland snubber for flying capacitor multilevel inverter and converter," *IEEE Trans. Ind. Electron.*, vol.51, no.6, pp.1290-1296, Dec 2004.

Poh Chiang Loh, D. G. Holmes, Y. Fukuta and T. A. Lipo, "Reduced common-mode modulation strategies for cascaded multilevel inverters," *IEEE Trans. Ind. Appl.*, vol. 39, no. 5, pp. 1386-1395, 2003.

Rodriguez, J., J.S. Lai and F.Z. Peng, "Multilevel inverters: A survey of topologies, controls and applications," *IEEE Trans. Ind. Electron.*, vol.49, no.4, pp.724-738, 2002.