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AN ARBITRARY SWITCHING HYBRID PULSE WIDTH MODULATION STRATEGY FOR THREE LEVEL INVERTERS

Bagya, B., Saranya, D., Vigneswari, A. and *Thamizharasan, S.

Department of Electrical and Electronics Engineering, Surya Group of Institutions, Vikravandi, Tamilnadu, India

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ABSTRACT

This paper presents an arbitrary switching hybrid pulse width modulation (ASHPWM) strategy for three level inverters. This hybrid-modulation strategy represents an amalgamation of fundamental-frequency modulation and sinusoidal pulse width modulation (SPWM) strategy and is designed for performance of the well-known carrier based modulation strategies. The main characteristic of this modulation is the reduction of switching losses with good harmonic performance, balanced power loss dissipation among the devices in the H- bridge inverter. PWM and its digital controller for PWM circulation are implemented on a Xilinx Spartan 3E-500 FG320 processor. The feasibility of this hybrid modulation is verified through simulation and experimental results.

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INTRODUCTION

In recent years, three level inverter shown in Fig.1 is widely used in industrial and domestic applications. Sinusoidal pulse width modulation (SPWM) methods are commonly employed in a full-bridge inverter to achieve lesser total harmonic distortion (THD) and reduced filter size. The well known switching schemes like unipolar PWM, bipolar PWM and other novel PWM strategies are widely used to extract variable voltage variable frequency (VVVF) for drive applications (Mohan *et al.*, 1995; Boost and Ziogas 1998; Holtz 1992). In Unipolar switching scheme the output voltage level changes between either 0 to $-V_d$ or from 0 to $+V_d$. This scheme 'effectively' has the effect of doubling the switching frequency as far as the output harmonics are concerned, compared to the bipolar- switching scheme. Similarly, In bipolar PWM output voltages voltage switches between two levels $-V_d$ and $+V_d$. In this scheme, the diagonally opposite transistors are turned on or turned off at the same time. For a full-bridge inverter with bipolar PWM scheme the output voltage is between $-V_d/2$ and $+V_d/2$. In this connection to improve output profile, the inverted sine carrier PWM (ISCPWM) control scheme for single-phase full-bridge inverter that eliminates poor output voltage spectral quality

and reduced fundamental output voltage. Still there is possibility to be done more than that in recent innovations, a new amplitude modulation triangular carrier. The peak of the triangular carrier is modulated to bring the instantaneous value of unit sine wave at that instant. Using this method, the three level inverter can be operated without entering into over modulation region. In these methods, the power devices are commutated at high frequency that results in high switching losses.

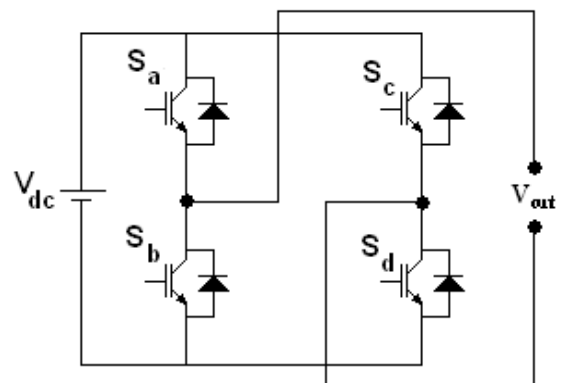


Fig. 1. Three Level inverter

*Corresponding author: Thamizharasan, S.

Department of Electrical and Electronics Engineering, Surya Group of Institutions, Vikravandi, Tamilnadu, India.

Later to overcome this drawback, soft-switching techniques have been proposed in recent years (Lai 1997; Chan et al., 1997), thereby decreasing switching losses. However, the soft-switching methods require auxiliary switches, diodes with higher ratings than those of main switches and it depends upon the specific design. These methods may increase the voltage or current stresses on these main switches and it includes duty ratio limitation, load-type restrictions. An additional alternative is hybrid PWM (HPWM) proposed in (Lai and Ngo1995) without significant switching loss and thermal management (Jeevananthan et al., 2004) from which a high-quality output waveform can be obtained. With this method, only two of the the four power switches are commutated at high frequency. With the aid of this method, total switching loss is reduced and the switching losses of the four switches become unequal, particularly at higher frequency or heavy load. This results excessive heating of the two high-frequency switches and it degrades system reliability. This paper introduces arbitrary switching hybrid pulse width modulation (ASHPWM) strategy for balancing power losses among the devices in the H- bridge inverter. This hybrid-modulation strategy incorporates fundamental-frequency modulation and modified carrier pulse width modulation (PWM) strategy and is designed for performance of the well-known carrier based modulation strategies.

Proposed arbitrary switching hybrid-modulation strategy

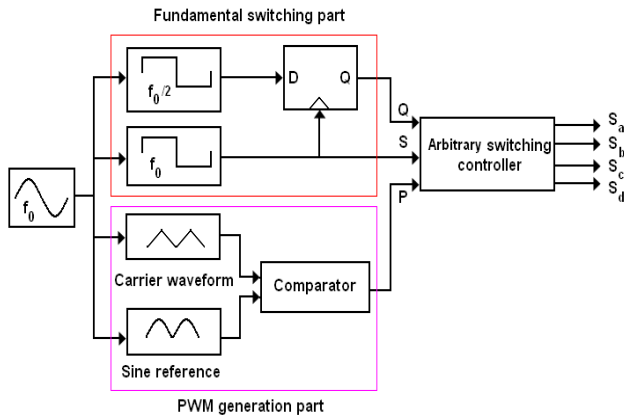


Fig. 2. Block diagram of arbitrary switching hybrid modulation method

The proposed arbitrary switching hybrid pulse width modulation (ASHPWM) strategy shown in Fig. 2 is the amalgamation of fundamental frequency switching (FFS) as encircled by red color and carrier based PWM generation for VVVF operation, as a result that the output acceded to the texture of switching-loss reduction from FPWM and good harmonic performance from carrier based PWM. The arbitrary switching controller basically consists of combinational logic circuits generate gating signal for each devices with two different frequencies, two being switched at FFS, while the other two switches are modulated at PWM, for simplicity therefore the resultant switching patterns are the same as those obtained with SPWM. The input signals for this controller are Q, S and P. The signal Q is obtained from D flip flop. The square wave signal of half the fundamental frequency ($f_0/2$) with 50% duty Cycle and the fundamental frequency signal (f_0) are considered as inputs to the data and clock pins of the D-

type flip-flop, respectively. FFS (S) is a square wave signal in phase with the modulating waveform, when $S = 1$ during the positive half cycle of the modulating signal, and $S = 0$ during negative half cycle. The signal (P) is obtained by direct comparison of rectified sine modulating signal with any modified carrier functions. The signal (Q) formulates every power switch operating at PWM, and FFS arbitrary to equalize the power losses among the devices. The logical functions used in arbitrary switching controller are expressed in equation (1) to (4).

$$S_a = QSP + \bar{Q}\bar{S} \tag{1}$$

$$S_b = Q\bar{S}P + \bar{Q}S \tag{2}$$

$$S_c = \bar{Q}\bar{S}P + Q\bar{S} \tag{3}$$

$$S_d = \bar{Q}SP + QS \tag{4}$$

Fig.4 depicts that each gate signal is composed of both low- and high-frequency signals. If $Q=0$, S_a and S_b are commutated at low frequency while S_c and S_d are commutated at high frequency. If $Q=1$, S_a and S_b are commutated at high frequency, while S_c and S_d are commutated at low frequency. Since Q is a random signal, the average switching frequency among the four switches is equalized. Voltage stress and current stress of four switches are also equalized. The proposed power balance method allows use of identical power devices and heat sinks, permitting a simpler, more reliable, design.

Simulation and experimental results

In order to show the feasibility of the proposed modulation method, the simulation study was performed by using MATLAB/Simulink software with dc-link voltage (V_{dc}) = 100V, switching frequency of PWM signal (f_s)= 1kHz, Fundamental frequency (f_0)=50Hz, $R=150\Omega$ and $L=106mH$ respectively. SPWM chosen as a control strategy to show the feasibility of the proposed controller. The gating signals for each devices and the corresponding output voltage are pictured in Figs. 3 and 4 respectively.

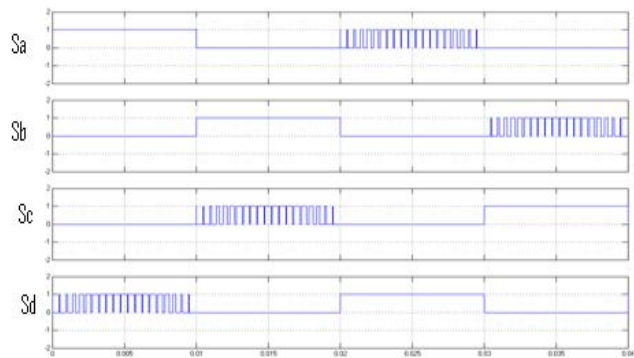


Fig. 3. Pulse generation using proposed method

Fig.5 and Fig.6 shows the performance comparison between the modulation strategies. Fig. 3 shows the variation of fundamental output voltage against modulation depth .In this, it is inferred that at low modulation depth, ISCPWM gives more fundamental output voltage compared to unipolar and

AMTCPWM method. The fact is due to increased pulse width in the ISCPWM for the given low modulation depth. Fig (4) depicts the variation of fundamental output voltage (THD) against modulation. ISCPWM shows the good harmonic profile over the entire range of modulation depth except at modulation closer to 1.

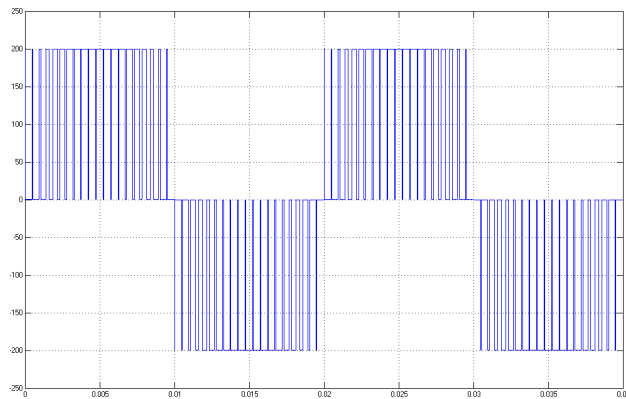


Fig. 4. Output voltage for SPWM using proposed method

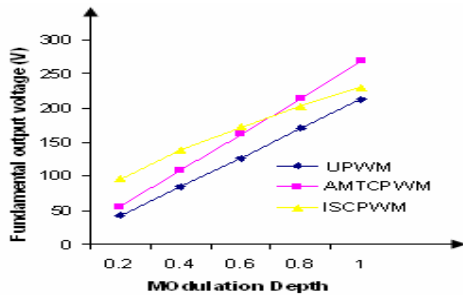


Fig. 5. Variation of fundamental output voltage against modulation depth

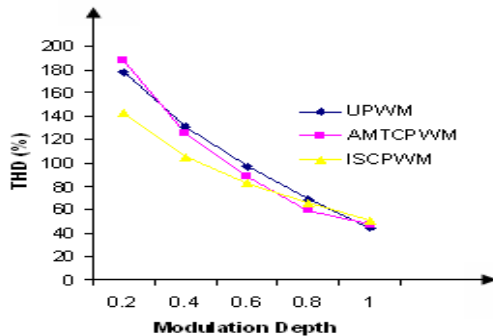


Fig. 6. Variation of THD against modulation depth

The block diagram of the proposed controller shown in Fig. 2 is implemented for a three-level inverter is represented in Fig. 7. The inverter shown in Fig. 1 is fabricated using similar specification as those used in simulation. Xilinx Spartan 3E-500 FG320 processor is chosen for implementing proposed algorithm and it is reconfigurable device unit that utilize dedicated flip flops and logical gates. It is evident from the Fig. 8, the fact that the same output is obtained using simulation and hardware highlights the practical feasibility of the proposed digital PWM controller.



Fig. 7. Experimental setup

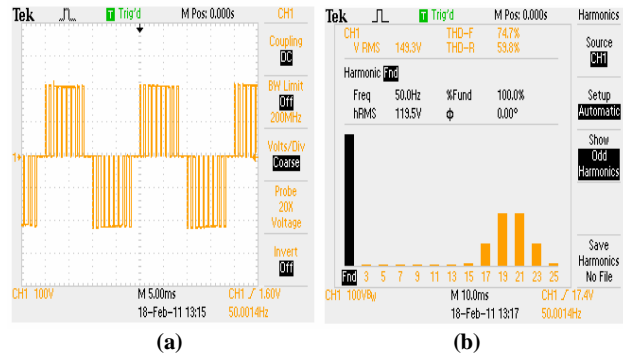


Fig. 8 (a). Output voltage waveform (b) Harmonic spectrum

Conclusion

The proposed arbitrary switching hybrid pulse width modulation (ASHPWM) strategy for full-bridge inverters shows the advantage of thermal equalization, and verifies the feasibility and practicality of the digital design. It is compact and easily realized, particularly when the inverter is controlled by a chip design methodologies.

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